IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	Law, Oscar Ming Kin	Examiner:	Tra, Anh Quan
Application No.:	10/820,556	Group Art Unit:	2816
Filed:	April 8, 2004	Docket No.:	00100.04.0002
For:	ADAPTIVE SUPPLY VOLTAGE BODY BIAS APPARATUS AND METHOD THEREOF		

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Sir:

Appellants submit this brief further to the Notice of Appeal filed June 30, 2008 (the "Notice of Appeal") in the above-identified application (the "Application").

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I. Real Party in Interest

ATI Technologies Inc. is the real party in interest in this appeal by virtue of an executed Assignment from the named Inventor of his entire interest to ATI Technologies Inc. The Assignment evincing such ownership interest was recorded on April 8, 2004, in the United States Patent and Trademark Office at Reel 015195, Frame 0963.

II. Related Appeals and Interferences

To Appellants' knowledge, there are no related Appeals or Interferences filed, pending, or decided.

III. Status of Claims

The originally filed Application contained claims 1-23, claim 24 was added by amendment in Appellants' Response to a non-final Office Action, mailed on April 5, 2005 and claim 25 was added by amendment in Appellants Response to a non-final Office Action mailed on March 3, 2006. Claims 2-6[1], 11, 21, 22 and 25 were subsequently canceled. Claims 1, 6, 10, 12, 13, 16, 19, 20 and 24 were amended during prosecution of the instant application. Claims 1, 7-10, 12-20, 23 and 24 are rejected[2]. No claims have been allowed and there are no objections to the claims. A copy of appealed claims 1, 7-10, 12-20, 23 and 24 are attached at Appendix A. Of the pending, appealed claims, claims 1, 10, 16, 20 and 24 are independent.

[1] Claims 5 and 6 were canceled by amendment after filing of the instant appeal under 37 C.F.R. § 41.33(a).

[2] Taking into account that claims 5 and 6 were canceled by the amendment under 37 C.F.R. § 41.33(a).

IV. Status of Amendments

A final Office Action was mailed November 9, 2007. In response, a Notice of Appeal, Pre-Appeal Brief Request For Review and Remarks For Pre-Appeal Brief Request For Review were filed by Appellant on February 11, 2008. Following a Notice Of Panel Decision from Pre-Appeal Brief Review mailed April 10, 2008, a non-final Office Action was subsequently mailed April 11, 2008 (the "Appealed Office Action"). Subsequent to the filing of the Notice of Appeal, an amendment under 37 C.F.R. § 41.33(a) was filed on August 27, 2008 canceling claims not affecting the scope of any other pending claim in this proceeding. The claims listed in Appendix A reflect the claims as they stood at the time the Appealed Office Action was mailed, with the exception of the claims canceled by the amendment under 37 C.F.R. § 41.33(a).

V. Summary of Claimed Subject Matter

As known in the art, integrated circuits may comprise different computing devices (e.g., logic gates comprising one or more transistors, etc.) operating in conjunction. As further known, such devices may be characterized, in part, by threshold voltages that affect the operating frequency of the device—lower threshold devices are capable of operating at faster speeds (but with higher leakage current) than devices having higher thresholds (but with lower leakage current). High leakage currents can lead to undesirably higher power consumption for integrated circuits. Thus, designers of integrated circuits often balance the desire for high frequency operation (using device having lower threshold voltages) against the need to minimize leakage currents.

Generally, the present invention is directed to the adaptive control of supply voltages and body biases for computing devices, implemented within an integrated circuit, each having different ones of a plurality of different threshold voltages, thereby providing control over performance and leakage currents. (Application, ¶¶ 0019-0021) In one embodiment, best illustrated in FIG. 1 (reproduced below), an adaptive supply voltage and body bias apparatus 100 comprises a master controller 102 that, in response to an operation state value 110, generates a supply voltage indicator 112 that is provided to a dynamic voltage supplier 104 (Application, ¶ 0023) and a body bias indicator 116 that is provided to an adaptive body biaser 106 (Application, ¶ 0024). In turn, the dynamic voltage supplier 104 provides a supply voltage 114 to multiple threshold devices 108 (Application, ¶ 0023), whereas the adaptive body biaser 106 provides a body bias voltage 120 to the multiple threshold devices 108 (Application, ¶ 0024).

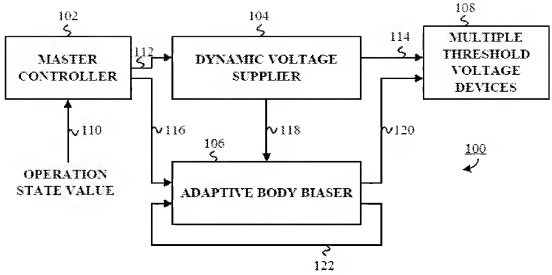

FIG. 1

In another embodiment, best illustrated in FIG. 3 (reproduced below), the apparatus 138 is essentially the same as the apparatus 100 disclosed in FIG. 1, with the addition of a frequency monitor 142. The frequency monitor 142 receives an output frequency indicator 140 from the multiple threshold voltage devices 108 (Application, ¶ 0028) as well as a reference frequency indicator 146 corresponding to optimized performance (Application, ¶ 0029). The frequency monitor 142 generates a frequency offset value 144 based on a comparison of the output frequency indicator 140 and the reference frequency indicator 146. (Id.) In response, the master controller 102 generates second supply voltage and body bias indicators 112, 116, respectively, that, in turn cause the dynamic voltage supplier 104 and adaptive body biaser 106 to provide second supply and body bias voltages 114, 120, respectively, to the multiple threshold voltage devices 108, thereby tuning operating efficiency of the multiple threshold voltage devices 108. (Application, ¶¶ 0030, 0031)

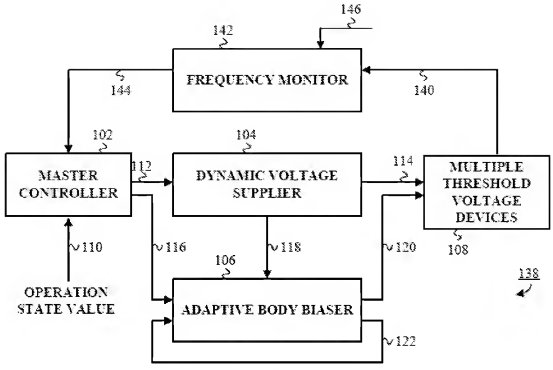

FIG. 3

Claim 1 recites an adaptive supply voltage and body bias apparatus (FIG. 1, 100; FIG. 3, 138) that includes a master controller (FIGs. 1 & 3, 102; ¶¶ 0022, 0023, 0027, 0030) operatively responsive to an operation state value (FIGs. 1 & 3, 110; ¶¶ 0019, 0022). The master controller is operably coupled to a dynamic voltage supplier that receives a supply voltage indicator from the master controller (FIGs. 1 & 3, 104; ¶¶ 0020, 0023), and to an adaptive body biaser that receives a body bias indicator from the master controller (FIGs. 1 & 3, 106; ¶¶ 0020, 0024). In turn, a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, are configured receive a supply voltage from the dynamic voltage supplier and to receive at least one body bias voltage from the adaptive body biaser (FIG.2, 130-134; ¶ 0026; FIGs. 1 & 3, 108; ¶¶ 0021, 0024). The master controller is operative to generate a second supply voltage indicator and a second body bias indicator based on a difference between optimized performance and actual performance of the plurality of

computing devices (¶ 0029), and to provide the second supply voltage indicator to the dynamic voltage supplier and the second body bias indicator to the adaptive body bias circuit (¶ 0030).

Claim 10 recites a method for providing an adaptive supply voltage and body bias voltage in which a supply voltage indicator and a body bias indicator are generated in response to an operation state value (FIG. 7, 202; ¶ 0038). Thereafter, a supply voltage is generated in response to the supply voltage indicator (FIG. 7, 204; ¶ 0038) and at least one body bias voltage is generated in response to the body bias indicator (FIG. 7, 204; ¶ 0038). Both the supply voltage and the at least one body bias voltage are provided to each of a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages (FIG. 7, 208; ¶ 0039). At least one of the plurality of computing devices generates an output frequency indicator (¶ 0028; FIG. 3, 140) that is provided to a frequency monitor (¶ 0028; FIG. 3, 142; FIG. 5; ¶ 0034). The frequency monitor then generates a frequency offset value based on the output frequency indicator and a reference frequency (¶ 0029; FIG. 3, 144).

Claim 16 recites an adaptive supply voltage and body bias apparatus (FIG. 1, 100; FIG. 3, 138) that includes a master controller (FIGs. 1 & 3, 102; ¶¶ 0022, 0023, 0027, 0030) operative to receive an operation state value (FIGs. 1 & 3, 110; ¶¶ 0019, 0022) and generate a supply voltage indicator and a body bias indicator based on the operation state value (FIG. 7, 202; ¶ 0038). The master controller is operably coupled to a dynamic voltage supplier that receives a supply voltage indicator from the master controller (FIGs. 1 & 3, 104; ¶¶ 0020, 0023), and to an adaptive body biaser that receives a body bias indicator from the master controller (FIGs. 1 & 3, 106; ¶¶ 0020, 0024). In turn, a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, are configured receive a supply voltage from the dynamic voltage supplier and to receive at least one body bias voltage

from the adaptive body biaser (FIG.2, 130-134; ¶ 0026; FIGs. 1 & 3, 108; ¶¶ 0021, 0024). A frequency monitor is operably coupled to the plurality of computing devices and receives an output frequency indicator from at least one of the plurality of computing devices (FIG. 3, 142; ¶ 0028, 0029; FIG. 5; ¶ 0034).

Claim 20 recites a method for tuning a supply voltage and a body bias for a processing device. For each sub-section of a plurality of sub-sections of the processing device, each sub-section including a plurality of computing devices having a different one of a plurality of threshold voltages relative to the other sub-sections (FIG. 2; ¶ 0026), the method includes generating a supply voltage indicator and a body bias indicator in response to an operation state value (FIG. 7, 202; ¶ 0038). Thereafter, a supply voltage is generated in response to the supply voltage indicator (FIG. 7, 204; ¶ 0038) and at least one body bias voltage is generated in response to the body bias indicator (FIG. 7, 204; ¶ 0038). Both the supply voltage and the at least one body bias voltage are provided to each of the plurality of computing devices (FIG. 7, 208; ¶ 0039). At least one of the plurality of computing devices generates an output frequency indicator (¶ 0028; FIG. 3, 140). A frequency monitor (¶ 0028; FIG. 3, 142; FIG. 5; ¶ 0034) then generates a frequency offset value based on the output frequency indicator and a reference frequency (¶ 0029; FIG. 3, 144). Finally, the supply voltage and the body bias voltage are updated in response to the frequency offset value and the operation state value (¶ 0030).

Claim 24 recites an adaptive supply voltage and body bias apparatus (FIG. 1, 100; FIG. 3, 138) that includes a dynamic voltage supplier operative to receive a supply voltage indicator (FIGs. 1 & 3, 104; ¶¶ 0020, 0023) and an adaptive body biaser operative to receive a body bias indicator (FIGs. 1 & 3, 106; ¶¶ 0020, 0024). In turn, a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, are

configured receive a supply voltage from the dynamic voltage supplier and to receive at least one body bias voltage from the adaptive body biaser (FIG.2, 130-134; ¶ 0026; FIGs. 1 & 3, 108; ¶¶ 0021, 0024). The plurality of computing devices comprise a first computing device (FIG. 6, 180; ¶ 0035) and a second computing device (FIG. 6, 182; ¶ 0036), wherein each of the first computing device and the second computing device comprises at least two transistor devices operatively coupled in a push-pull configuration (FIG. 6, 188, 190, 196, 198), and wherein an output of the first computing device is operatively coupled to an input of the second computing device (FIG. 6, 192).

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1, 7-10, 12-20, 23 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable given Katoh et al. (U.S. Patent No. 6,380,764; hereinafter "Katoh") in view of Miyazaki et al. (U.S. Patent No. 6,774,705; hereinafter "Miyazaki").

VII. Argument

A. Rejection of Claims 1, 7-10, 12-20, 23 and 24 Under 35 U.S.C. 103(a) Based On Katoh In View Of Miyazaki

1. Brief Summary Of The Katoh Reference

Katoh is generally directed to the problem common to integrated circuits of balancing the desire to have low threshold/high speed devices, but that have significant leakage current with the use of high threshold/low speed devices that offer significantly reduced leakage currents. (col. 2, lines 9-63) To address this situation, Katoh teaches the provision of multiple threshold switching devices (i.e., low and high threshold MOSFETs) such that signal paths having varying delays and varying levels of leakage current may be provided. (col. 3, lines 25-37) More significantly, Katoh teaches that such high and low threshold switching devices may be mixed so as to meet any necessary speed requirements (i.e., set maximum delays such that a minimum operation frequency is achieved) without needlessly incurring leakage currents by making all of the switching devices low threshold devices. (col. 3, lines 38-51) Given this capability to design signal paths using either or both of the low and high threshold devices, Katoh further discloses methods whereby circuits meeting desired switching speeds, but still maximizing any possible reduction in current leakage, may be obtained by selectively combining low and high threshold devices during the design phase of the circuit. (col. 4, line 48 – col. 5, line 9) Thus, Katoh is seen to provide a system wherein tradeoffs between switching speeds (or delays) and leakage current can be designed into a circuit with greater precision, thereby maximizing the benefits of low and high threshold devices. In keeping with these teachings, Katoh is silent with regard to

the possibility of dynamically controlling the supply/bias voltages to the multiple threshold devices.

2. Brief Summary Of The Miyazaki Reference

Generally, Miyazaki teaches a semiconductor integrated circuit that is provided with control circuits (FIG. 14; VDDGEN, VBBGEN, FRQGEN) for controlling a power supply voltage (e.g, N12), a substrate bias voltage (e.g., N13) and a clock frequency (e.g., N11) for the semiconductor integrated circuit (LSI) or multiple blocks thereof (FIG. 24; LSI20-LSI40). As shown, for example, in the embodiment of Miyazaki's FIG. 14, the control circuitry includes a monitor (MON) that monitors the power supply voltage (N12), substrate bias voltage (N13) and clock frequency (N11). A comparator (CMP) compares the clock frequency with a reference signal (REF) and causes either an up signal (N15) or a down signal (N16) to be issued, thereby causing a decoder (DEC) to issue a decoder signal (N17) that causes corresponding adjustments in the control circuits (VDDGEN, VBBGEN, FRQGEN). (See also, col. 10, lines 15-42) In another embodiment, the integrated circuit (LSI) can be divided into separate blocks (LSI20-LSI40) each requiring correspondingly separate power supply voltages, body bias voltages and clock frequencies (FIG. 24; col. 13, lines 29-45).

3. Claims 1, 7-10, 12-20, 23 and 24

With reference, for example, to claim 1, the Appealed Office Action notes that Katoh teaches a delay circuit (Katoh, FIG. 12, inv1 & inv2) comprising computing devices having different ones of a plurality of different threshold voltages (Appealed Office Action, Detailed Action, p. 2). To this end, Miyazaki is cited for the teachings of a control circuit, capable of controlling both supply voltages and body bias voltages for an integrated circuit, that may

allegedly be used to "provide a precise delay due to temperature/process variation." (Id.) Thus, it is reasoned, those of ordinary skill in the art would be motivated to combine the teachings of Miyazaki with those of Katoh "in order to [maintain] an accurate delay for circuits INV1 and INV2."[3] (Id.) While Appellant traverses the assertion that the combination of Katoh in view of Miyazaki teaches all of the claimed limitations of the appealed claims, Appellant respectfully submits (even assuming, for the sake of argument, that all claim limitations are met) that the combination of Katoh and Miyazaki is improper for the reasons stated below.

a. The combination of Katoh in view of Miyazaki is improper because it is contrary to teachings in Katoh against the proposed combination

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. (M.P.E.P. § 2141.02(VI), *quoting W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984) (emphasis in original)) Where there is a teaching away, "[i]t is

[3] In Appellant's Remarks For Pre-Appeal Brief Request For Review filed February 11, 2008 (the "Remarks"), four separate arguments against the combination of Katoh in view of Miyazaki were set forth, which Appellant notes are substantially identical to the arguments presented in the instant appeal. Despite this, Appellant further notes that the rationale for combining Katoh and Miyazaki in the two cited quotes constitutes the sole difference between the final Office Action mailed November 9, 2007 and the Appealed Office Action—the basis for rejecting the claims between these two Office Actions is otherwise verbatim identical. While this modification to the motivation to combine arguably addresses (but does not, in Appellant's view, overcome) one of Appellant's arguments presented in the Remarks, the Appealed Office Action is completely silent on the other three arguments. Appellant respectfully submits that this failure to respond to various ones of Appellant's previously presented argument violates both the Office's general goal to achieve "compact prosecution" (M.P.E.P. § 2106(II): "It is essential that patent applicants obtain a prompt yet complete examination of their applications.") and its specific instruction to answer an applicant's arguments (M.P.E.P. §707.07(f): "Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.").

improper to combine references where the references teach away from their combination." (M.P.E.P. § 2145(X)(D)(2))

The suggested combination of Katoh and Miyazaki is improper because Katoh expressly teaches away from the suggested combination. In particular, Applicant notes col. 1, line 52 – col. 2, line 63 of Katoh, where the possibility of controlling body bias voltages, particularly where multiple threshold voltage devices are provided, in order to reduce leakage current was considered by Katoh. However, as the cited passage makes perfectly clear, particularly in light of the subsequent teachings, Katoh specifically rejected an adaptive control approach in favor of provision of multiple threshold devices that may be configured at the time of circuit design to provide delay paths that meet the necessary speeds, but that also minimize the number of devices having high leakage current. In light of this, it is improper to combine the control circuitry of Miyazaki with the multiple threshold devices of Katoh, as asserted in the Appealed Office Action, because Katoh clearly teaches away from such a combination. For this reason, the combination of Katoh in view of Miyazaki is improper, and the rejection of the pending claims on this basis should be overturned.

b. The combination of Katoh in view of Miyazaki is improper because it would change an operating principle of Katoh

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. (M.P.E.P. § 2143.01(VI))

Ignoring for the moment the express teachings of Katoh against the suggested combination, Appellant respectfully asserts that one having ordinary skill in the art would not be motivated to combine the multiple threshold devices of Katoh with the control circuitry taught by

Miyazaki because to do so would change a basic operating principle of Katoh. As recited above, Katoh balances the conflicting requirements of speed versus current leakage by providing enough multiple threshold devices such that the delays in any given signal path may be specified at the time of circuit design without incurring more than the necessary amount of leakage current. As a result, one having ordinary skill in the art would not be motivated to adjust delay values using the control circuitry of Miyazaki because to do so would interfere with the desired speed versus leakage current balance provided during the circuit's design. Stated another way, a person of ordinary skill in the art would not combine the teachings of Miyazaki with those of Katoh because to do so would change the basic operating principle of Katoh.

In response to this argument, in the Office Action mailed November 9, 2007 (Response to Arguments, § 5) it is asserted that, in essence, Katoh teaches a delay circuit having multiple threshold devices and Miyazaki teaches a control circuit for controlling a similar type of delay circuit; therefore, if one wants to control the delays of Katoh's delay circuit, one would be motivated to employ Miyazaki's control circuitry. However, this line reasoning simply assumes the conclusion being argued against and ignores the purpose of Katoh described above (in addition to ignoring Katoh's express rejection of such a combination, as noted above), i.e., that Katoh seeks to balance the speed versus leakage current trade off at the time a circuit is designed. (Katoh, col. 2, lines 60-63; col. 3, lines 8-12) For this reason, the combination of Katoh in view of Miyazaki is improper, and the rejection of the pending claims on this basis should be overturned.

c. The combination of Katoh in view of Miyazaki is improper because it would obviate the very purpose of Katoh and would have no reasonable expectation of success

M.P.E.P. § 2143.01(V) states that the proposed modification to a reference cannot render that reference unsatisfactory for its intended purpose. Additionally, a modification to a reference is proper only when there is a reasonable expectation of success. (M.P.E.P. § 2143.02)

The combination of Katoh and Miyazaki is improper to the extent that the resulting device would be so complex as to be impractical, thereby obviating the very purpose of Katoh and possessing little likelihood of success. As noted above, Katoh provides multiple threshold devices to allow a designer to design a circuit meeting the necessary speed requirements while simultaneously minimizing the number of high leakage gates employed. Because the high and low threshold gates illustrated in Katoh are not combined until such time as the circuit is designed according to the designated speed and leakage current requirements, it would be necessary to duplicate the control circuitry of Miyazaki for virtually every gate within Katoh's device since it would be impossible to know ahead of time how Katoh's gates would be combined. Such duplication of circuitry, even assuming that it is technically feasible, would necessarily make the resulting device exceeding complex and therefore unlikely to be used in practice. For this reason, the combination of Katoh in view of Miyazaki is improper, and the rejection of the pending claims on this basis should be overturned.

d. The combination of Katoh in view of Miyazaki is improper because one of ordinary skill in the art would not be motivated to combine the references

In its *KSR* decision (*KSR International Co. v. Teleflex, Inc.*, 550 U.S. ____, 82 USPQ2d 1385 (2007)), with regard to motivation to combine the references, the United States Supreme Court, noted that "market forces" may provide sufficient motivation for making variations to

prior art teachings. (*Id.* at ____, 82 USPQ2d at 1396) However, by implication, it must also be true that variations to prior art teachings that would run counter to such "market forces" would not be evident to practitioners in the art, thereby cutting against any motivation to combine such prior art teachings.

Appellant respectfully submits that the cited combination of Katoh and Miyazaki runs counter to the market forces applicable to devices of the type described by Katoh and Miyazaki. In particular, both Katoh and Miyazaki concern integrated circuits. It is widely known in the art of integrated circuits that complexity and cost go hand in hand—increased complexity of an integrated circuit translates directly into increased costs to eventual purchasers of such devices. As described above, the combination of Miyazaki's control circuitry with the multiple threshold devices of Katoh would result in an device of such increased complexity as to make the resulting cost increase prohibitive. In this light, the conjecture that one of skill in the art would be motivated to combine Miyazaki's alleged ability to control delays via supply and body bias voltages with the multiple threshold voltage delay devices of Katoh in order to control the delays of Katoh's devices is not sufficient to overcome the certainty that the proposed changes would result in a device that is inordinately expensive, and therefore unlikely to achieve market success. For this reason, the combination of Katoh in view of Miyazaki is improper, and the rejection of the pending claims on this basis should be overturned.

VIII. Conclusion

For the reasons advanced above, Appellants submit that the Examiner erred in rejecting pending claims 1, 7-10, 12-20, 23 and 24 and respectfully request reversal of the decision of the Examiner.

Respectfully submitted,

Date: August 29, 2008

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APPENDIX A

CLAIMS ON APPEAL

1. An adaptive supply voltage and body bias apparatus comprising:

a master controller operatively responsive to an operation state value;

a dynamic voltage supplier operably coupled to the master controller, the dynamic voltage supplier operative to receive a supply voltage indicator from the master controller;

an adaptive body biaser operably coupled to the master controller, the adaptive body biaser operative to receive a body bias indicator from the master controller; and

a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, each of the plurality of computing devices being operative to receive a supply voltage from the dynamic voltage supplier and the plurality of computing devices being operative to receive at least one body bias voltage from the adaptive body biaser;

wherein the master controller further generates a second supply voltage indicator and a second body bias indicator based on a difference between optimized performance and actual performance of the plurality of computing devices, the master controller operative to provide the second supply voltage indicator to the dynamic voltage supplier and operative to provide the second body bias indicator to the adaptive body bias circuit.

7. The adaptive supply voltage and body bias apparatus of claim 1 wherein the master controller receives the operation state value from a processing device.

8. The adaptive supply voltage and body bias apparatus of claim 1 wherein the plurality of computing devices are disposed on a processing element.

9. The adaptive supply voltage and body bias apparatus of claim 1 wherein the supply voltage indicator and the body bias indicator are voltages.

10. A method for providing an adaptive supply voltage and body bias voltage, the method comprising:

generating a supply voltage indicator and a body bias indicator in response to an operation state value;

generating a supply voltage in response to the supply voltage indicator;

generating at least one body bias voltage in response to the body bias indicator;

providing the supply voltage to each of a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, and providing the at least one body bias voltage to the plurality of computing devices;

generating an output frequency indicator from at least one of the plurality of computing devices;

providing the output frequency indicator to a frequency monitor; and

generating, by the frequency monitor, a frequency offset value based on the output frequency indicator and a reference frequency.

12. The method of claim 10 further comprising:

providing the frequency offset value to a master controller;

generating a second supply voltage indicator and a second body bias indicator in response to the frequency offset value and the operation state value; and

providing the second supply voltage indicator to a dynamic voltage supplier and the second body bias indicator to an adaptive body biaser.

13. The method of claim 12 further comprising:

generating a second supply voltage;

generating at least a second body bias voltage; and

providing the second supply voltage to each of the plurality of computing devices and providing at least the second body bias voltage to the plurality of computing devices.

14. The method of claim 10 further comprising:

receiving the operation state value from a processing device.

15. The method of claim 10 wherein the plurality of computing devices are disposed on a processing element.

16. An adaptive supply voltage and body bias apparatus comprising:

a master controller operative to receive an operation state value, the master controller operative to generate a supply voltage indicator and a body bias indicator based on the operation state value;

a dynamic voltage supplier operably coupled to the master controller, the dynamic voltage supplier operative to receive the supply voltage indicator;

an adaptive body biaser operably coupled to the master controller, the adaptive body biaser operative to receive the body bias indicator;

a plurality of computing devices, each of the computing devices having different ones of a plurality of threshold voltages, the plurality of computing devices operative to receive a supply voltage from the dynamic voltage supplier and a bias voltage from the adaptive body biaser;

a frequency monitor operably coupled to the plurality of computing devices, the frequency monitor operative to receive an output frequency indicator from at least one of the plurality of computing devices.

17. The adaptive supply voltage and body bias apparatus of claim 16 wherein the frequency monitor generates a frequency offset value based on a comparison of the output frequency indicator and a reference frequency indicator.

18. The adaptive supply voltage and body bias apparatus of claim 17 wherein the frequency offset value is provided to the master controller, the master controller generating a second supply voltage indicator and a second body bias indicator in response to the frequency offset value and the operation state value, the master controller operative to provide the second supply voltage indicator to the dynamic voltage supplier and operative to provide the second body bias indicator to the adaptive body bias circuit.

19. The adaptive supply voltage and body bias apparatus of claim 18 further comprising:

the plurality of computing devices operative to receive a second supply voltage from the dynamic voltage supplier and a second body bias voltage from the adaptive body biaser.

20. A method for tuning a supply voltage and a body bias for a processing device, the method comprising:

for each sub-section of a plurality of sub-sections of the processing device, wherein each sub-section includes a plurality of computing devices having a different one of a plurality of threshold voltages relative to the other sub-sections:

(a) generating a supply voltage indicator and a body bias indicator in response to an operation state value;

(b) generating a supply voltage in response to the supply voltage indicator;

(c) generating a body bias voltage in response to the body bias indicator;

(d) providing the supply voltage and the body bias voltage to a plurality of computing devices, each of the computing devices having one of a plurality of threshold voltages;

(e) generating an output frequency indicator with at least one of the plurality of computing devices;

(f) generating a frequency offset value based on the output frequency indicator and a reference frequency indicator; and

(e) updating the supply voltage and the body bias voltage in response to the frequency offset value and the operation state value.

23. The method of claim 22 wherein the operating state value may be one of a plurality of values for each of the sub-sections.

24. An adaptive supply voltage and body bias apparatus comprising:

a dynamic voltage supplier operative to receive a supply voltage indicator;

an adaptive body biaser operative to receive a body bias indicator; and

a plurality of computing devices, each of the computing devices having different ones of a plurality of different threshold voltages, each of the plurality of computing devices operative to receive a supply voltage from the dynamic voltage supplier and the plurality of computing devices being operative to receive at least one body bias voltage from the adaptive body biaser;

wherein the plurality of computing devices comprise a first computing device and a second computing device, wherein each of the first computing device and the second computing device comprises at least two transistor devices operatively coupled in a push-pull configuration, and wherein an output of the first computing device is operatively coupled to an input of the second computing device.

APPENDIX A

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS

[NONE]